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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/651,914	08/29/2003	Suan Jeung Boon	108298709US	9566	
25096	7590	06/15/2004	EXAMINER		
PERKINS COIE LLP				QUINTO, KEVIN V	
PATENT-SEA				ART UNIT	
P.O. BOX 1247				2826	
SEATTLE, WA 98111-1247				PAPER NUMBER	

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/651,914	BOON ET AL.
Examiner	Art Unit	
Kevin Quinto	2826	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### **Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 29 August 2003.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) \_\_\_\_\_ is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) 27-37 is/are allowed.

6)  Claim(s) 1-3,6,11,12,15,19-21,23,25 and 26 is/are rejected.

7)  Claim(s) 4,5,7-10,13,14,16-18,22 and 24 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a))

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date .

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .

5)  Notice of Informal Patent Application (PTO-152)

6)  Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Specification***

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Objections***

2. Claim 11 is objected to because of the following informalities: "at least a portion of the lead." Appropriate correction is required.
3. In claim 11, "a plurality of leads" is described, however the limitation "at least a portion of the lead" is directed to only one lead. The examiner believes that the phrase "at least a portion of the lead" was meant to be directed to *all of the leads* and has thus been interpreted in this manner.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 3, 11, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Chou (United States Patent Application Publication US 2002/0089025 A1).

6. In reference to claim 1, Chou (United States Patent Application Publication US 2002/0089025 A1) discloses a similar device. Figure 4 illustrates a packaged microelectronic device with an image sensor die (2) and a bond pad (not shown). The image sensor die (2) has an active area with a first side and a second side which is opposite to the second side. A radiation transmissive window is positioned over the active area. A lead (1, 12) is mounted to the second side of the image sensor die (2) and is electrically coupled to the bond pad.

7. With regard to claim 2, there is a casing (5) which is over the bond pad, at least a portion of the second side of the image sensor die (2), and at least a portion of the lead (1, 12).

8. In reference to claim 3, there is a casing (5) which is over the bond pad, at least a portion of the second side of the image sensor die (2), and at least a portion of the lead (1, 12). The lead (1, 12) has an end external to the casing (5).

9. In reference to claim 11, Chou (United States Patent Application Publication US 2002/0089025 A1) discloses a similar device. Figure 4 illustrates a packaged microelectronic device with an image sensor die (2) and a plurality of bond pads (not shown). The image sensor die (2) has an active area with a first side and a second side which is opposite to the second side. The plurality of bond pads are on the first side. A radiation transmissive member is positioned over the active area. A plurality of leads (1, 12) are mounted to the second side of the image sensor die (2) and are electrically coupled to the bond pads. There is a casing (5) which covers the bond pads, at least

a portion of the second side of the image sensor die (2), and at least a portion of the each of the leads (1, 12).

10. In reference to claim 12, the leads (1, 12) have an end external to the casing (5).

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 6, 15, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou (United States Patent Application Publication US 2002/0089025 A1) in view of Ochi et al. (USPN 5,708,293).

13. In reference to claim 6, Chou does not disclose the use of a lead-on-chip tape to secure the lead to the die. However the use of lead-on-chip tape (LOC) is well known in the art. Ochi et al. (USPN 5,708,293, hereinafter referred to as the "Ochi" reference) discloses that using lead-on-chip tape leads to a device having the benefits of a lower cost and increased reliability (column 14, lines 17-22). In view of Ochi, it would therefore be obvious to use lead-on-chip tape in the Chou device.

14. In reference to claim 15, Chou does not disclose the use of a lead-on-chip tape to secure the lead to the die. However the use of lead-on-chip tape (LOC) is well known in the art. Ochi (USPN 5,708,293) discloses that using lead-on-chip tape leads to a device having the benefits of a lower cost and increased reliability (column 14, lines 17-

22). In view of Ochi, it would therefore be obvious to use lead-on-chip tape in the Chou device.

15. In reference to claim 23, Chou does not disclose the use of a lead-on-chip tape to secure the lead to the die. However the use of lead-on-chip tape (LOC) is well known in the art. Ochi (USPN 5,708,293) discloses that using lead-on-chip tape leads to a device having the benefits of a lower cost and increased reliability (column 14, lines 17-22). In view of Ochi, it would therefore be obvious to use lead-on-chip tape in the Chou device.

16. Claims 19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou (United States Patent Application Publication US 2002/0089025 A1) in view of Ichikawa et al. (USPN 6,104,086) and further in view Murakawa et al. (JP 07-263607) and further in view of Bessho et al. (USPN 6,372,548 B2).

17. In reference to claim 19, Chou does not disclose the use of leads having an arcuate configuration or a J-shape. However the use of J-shaped leads is well known in the art. Ichikawa et al. (USPN 6,104,086, hereinafter referred to as the "Ichikawa" reference) discloses that using J-shaped leads results in a semiconductor device with a reduced mounting area (column 1, lines 38-43). Ichikawa discloses such an example in Murakawa et al. (JP 07-263607, hereinafter referred to as the "Murukawa" reference). Bessho et al. (USPN 6,372,548, hereinafter referred to as the "Bessho" reference) discloses that the reduction of the mounting area for a semiconductor device is a known goal in the semiconductor art (column 1, lines 22-24). In view of Ichikawa, Murukawa,

and Bessho, it would therefore be obvious to use leads having an arcuate configuration or a J-shape in order to attain the benefit of a reduced mounting area.

18. In reference to claim 25, Chou does not disclose the use of leads having an arcuate configuration or a J-shape. However the use of J-shaped leads is well known in the art. Ichikawa (USPN 6,104,086) discloses that using J-shaped leads results in a semiconductor device with a reduced mounting area (column 1, lines 38-43). Ichikawa discloses such an example in Murakawa (JP 07-263607). Bessho (USPN 6,372,548) discloses that the reduction of the mounting area for a semiconductor device is a known goal in the semiconductor art (column 1, lines 22-24). In view of Ichikawa, Murakawa, and Bessho, it would therefore be obvious to use leads having an arcuate configuration or a J-shape in order to attain the benefit of a reduced mounting area.

19. Claims 20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou (United States Patent Application Publication US 2002/0089025 A1) in view of Harnden et al. (United States Patent Application Publication US 2003/0062601 A1) and further in view McLellan (USPN 5,130,783).

20. In reference to claim 20, Chou does not disclose the use of leads having an L-shape. However the use of L-shaped leads is well known in the art. Harnden et al. (United States Patent Application Publication US 2003/0062601 A1, hereinafter referred to as the "Harnden" reference) shows a device with L-shaped leads in figure 5A. Harnden further discloses that using L-shaped leads results in a semiconductor device with a lower profile (p.13, paragraph 174). McLellan (USPN 5,130,783) discloses that semiconductor devices with a low profile are desirable in the semiconductor art (column

1, lines 10-12). In view of Harnden and McLellan, it would therefore be obvious to use L-shaped leads in order to attain the benefit of a low profile semiconductor device.

21. In reference to claim 26, Chou does not disclose the use of leads having an L-shape. However the use of L-shaped leads is well known in the art. Harnden (United States Patent Application Publication US 2003/0062601 A1) shows a device with L-shaped leads in figure 5A. Harnden further discloses that using L-shaped leads results in a semiconductor device with a lower profile (p.13, paragraph 174). McLellan (USPN 5,130,783) discloses that semiconductor devices with a low profile are desirable in the semiconductor art (column 1, lines 10-12). In view of Harnden and McLellan, it would therefore be obvious to use L-shaped leads in order to attain the benefit of a low profile semiconductor device.

### ***Allowable Subject Matter***

22. Claims 27-37 are allowed.

23. Claims 4, 5, 7, 8, 9, 10, 13, 14, 16, 17, 18, 22, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a fabrication process for a semiconductor image sensor device that has a window fabricated onto a light sensitive region of the image sensor die via an adhesive film while a leadframe is

mounted to the bottom of the image sensor die such that a casing partially envelopes the leads.

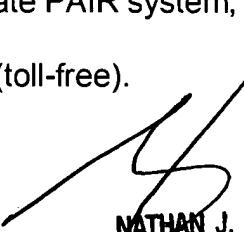
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ



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